IN THE CLAIMS

Please cancel claims 1-5 and 27-70 without prejudice.

Please amend claims 6, 9-12, 14-16, and 19-26 as follows below.

Please add new claims 71-90 as follows below.

MARKED-UP LISTING OF CLAIMS

1-5. (Cancelled)

6. (Currently Amended) A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects having at least two metal routing ~~on one or more~~ layers;

accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of ~~one or more~~ partitions, and the plurality of objects of the IC design are among the first plurality of ~~one or more~~ partitions; and

forming a second level for the IC design, including:

partitioning the [[second]] first level of the IC design into a second plurality of partitions, wherein one or more partitions of the first plurality of

partitions is represented by at least two partitions of the second plurality of partitions; and

within each partition of the second plurality of partitions, interconnecting objects substantially independently of other partitions of the second plurality of partitions using the at least two metal routing layers.

7. (Original) The method of claim 6, wherein the routing is multithreaded at least at a first time.

8. (Original) The method of claim 6, wherein the routing is single threaded at least at a first time.

9. (Currently Amended) The method of claim 6, wherein one or more partitions of the first plurality of ~~one or more~~ partitions has no objects of the plurality of objects.

10. (Currently Amended) The method of claim 6, wherein every partition of the first plurality of ~~one or more~~ partitions has one or more objects of the plurality of objects.

11. (Currently Amended) The method of claim 6, wherein

the interconnecting of objects substantially independently is subject ~~at least~~ to boundary conditions of the second plurality of partitions.

12. (Currently Amended) The method of claim 6, wherein the interconnecting of objects substantially independently is subject ~~at least~~ to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions.

13. (Original) The method of claim 6, wherein each partition of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions.

14. (Currently Amended) The method of claim 6, wherein each of the first level [[,]] and the second level of the IC design includes the at least two metal routing layers.

15. (Currently Amended) The method of claim 6, wherein

~~each of~~ the first level ~~, and the second level~~ of the IC design at least includes one layer of the at least two metal routing layers, and

the second level of the IC design includes the at least two metal routing layers.

16. (Currently Amended) A method of routing an integrated circuit (IC) design, comprising:

accessing the IC design including a plurality of objects having at least two metal routing ~~on one or more~~ layers;

accessing a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of ~~one or more~~ partitions, and the plurality of objects of the IC design are among the first plurality of ~~one or more~~ partitions; and

forming a second level for the IC design, including:

partitioning the [[second]] first level into a second plurality of partitions, wherein one or more partitions of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions;

allotting the second plurality of partitions among a plurality of areas, such that each area of the

plurality of areas includes one or more partitions of the second plurality of partitions; and

within each area of the plurality of areas, interconnecting objects substantially independently of other areas of the plurality of areas using the at least two metal routing layers.

17. (Original) The method of claim 16, wherein the routing is multithreaded at least at a first time.

18. (Original) The method of claim 16, wherein the routing is single threaded at least at a first time.

19. (Currently Amended) The method of claim 16, wherein

one or more partitions of the first plurality of ~~one or more~~ partitions has no objects of the plurality of objects.

20. (Currently Amended) The method of claim 16, wherein

every partition of the first plurality of ~~one or more~~ partitions has one or more objects of the plurality of objects.

21. (Currently Amended) The method of claim 16, wherein

the interconnecting of objects substantially independently is subject ~~at least~~ to boundary conditions of the second plurality of partitions.

22. (Currently Amended) The method of claim 16, wherein

the interconnecting of objects substantially independently is subject ~~at least~~ to boundary conditions of the plurality of areas.

23. (Currently Amended) The method of claim 16, wherein

the interconnecting of objects substantially independently is subject ~~at least~~ to a first partition of the second plurality of partitions locking at least a net shared by at least the first partition and a second partition of the second plurality of partitions to prevent a change of the net by the second partition of the second plurality of partitions.

24. (Currently Amended) The method of claim 16, wherein

the interconnecting of objects substantially independently is subject ~~at least~~ to a first area of the plurality of areas locking at least a net shared by at least the first area and a second area of the plurality of areas to prevent a change of the net by the second area of the plurality of areas.

25. (Currently Amended) The method of claim 16, wherein

each of the first level [[,]] and the second level of the IC design includes the at least two metal routing layers.

26. (Currently Amended) The method of claim 16, wherein

~~each of~~ the first level of the IC design ~~, and the second level~~ at least includes one layer of the at least two metal routing layers, and

the second level of the IC design includes the at least two metal routing layers.

27-70. (Cancelled)

71. (New) The method of claim 6, wherein

the plurality of objects are cells of an IC cell library.

72. (New) The method of claim 6, wherein the interconnecting of objects is a graph based routing.

73. (New) The method of claim 6, wherein the interconnecting of objects is a combination of an area based routing and a graph based routing.

73. (New) The method of claim 6, wherein the interconnecting of objects within the second plurality of partitions is a graph based routing, the interconnecting of objects between the second plurality of partitions is an area-based routing, and the interconnecting of objects between the first plurality of partitions is an area-based routing.

74. (New) The method of claim 6, further comprising: prior to the interconnecting of objects in each partition of the second plurality of partitions at the second level, forming a third level of the IC design, including

partitioning the second level of the IC design into a third plurality of partitions, wherein one or more partitions of the second plurality of partitions is represented by at least two partitions of the third plurality of partitions; and

within each partition of the third plurality of partitions, interconnecting objects substantially independently of other partitions of the third plurality of partitions using the at least two metal routing layers.

75. (New) The method of claim 74, further comprising:

after the interconnecting of objects in each partition of the second plurality of partitions at the second level,

within each partition of the first plurality of partitions at the first level, interconnecting objects substantially independently of other partitions of the first plurality of partitions using the at least two metal routing layers.

76. (New) The method of claim 6, wherein the at least two metal routing layers are an alloy.

77. (New) The method of claim 6, wherein

at least two partitions of the first plurality of partitions have differing shapes or sizes.

78. (New) The method of claim 16, wherein the plurality of objects are cells of an IC cell library.

79. (New) The method of claim 16, wherein the interconnecting of objects is an area-oriented graph based routing by an area-oriented multi-threaded graph-based detail router.

80. (New) The method of claim 16, wherein the interconnecting of objects is a combination of a grid based routing by a grid based router and a graph based routing by a graph based router.

81. (New) The method of claim 16, wherein the at least two metal routing layers are an alloy.

82. (New) The method of claim 16, wherein at least two partitions of the first plurality of partitions have differing shapes or sizes.

83. (New) A method of routing an integrated circuit (IC) design, comprising:

parsing IC design information including a plurality of cells of a cell library to support at least two metal wire routing layers for the IC design;

receiving a design netlist to access a first level for the IC design, wherein the first level of the IC design is partitioned into a first plurality of partitions, and the plurality of cells of the IC design are among the first plurality of partitions;

generating a topological wiring between the first plurality of partitions at the first level of the IC design using at least one layer of the at least two metal wire routing layers; and

forming a second level for the IC design, including

partitioning the first level of the IC design into a second plurality of partitions, wherein each of the first plurality of partitions is represented by at least two partitions of the second plurality of partitions,

generating a wiring between the second plurality of partitions at the second level of the IC design using at least one layer of the at least two metal wire routing layers, and

generating a detailed wiring using a graph-based routing within each of the second plurality of partitions to interconnect the cells substantially independently of other partitions of the second plurality of partitions using the at least two metal wire routing layers.

84. (New) The method of claim 83, wherein the IC design information of the cells includes a blockage within a first cell, and the generating of the detailed wiring using the graph-based routing is responsive to the blockage within the first cell.

85. (New) The method of claim 83, wherein the at least two metal wire routing layers are an alloy.

86. (New) The method of claim 83, wherein at least two partitions of the first plurality of partitions have differing shapes or sizes.

87. (New) The method of claim 83, wherein

the topological wiring between the first plurality of partitions at the first level of the IC design is generated using an area based global routing.

88. (New) The method of claim 83, wherein

the topological wiring between the first plurality of partitions at the first level of the IC design is generated using a grid-based global routing.

89. (New) The method of claim 88, wherein

the wiring between the second plurality of partitions at the second level of the IC design is generated using the grid-based global routing.

90. (New) The method of claim 88, wherein

the wiring between the second plurality of partitions at the second level of the IC design is generated using the graph-based routing.